Amendment to the Claims

The listing of claims will replace all prior versions, and listings of claims in the application.

1. (currently amended) A system comprising

a circuit;

an electrostatic discharge (ESD) protection system; and

a pad,

wherein the ESD protection system substantially eliminates ESD from flowing from the pad into the circuit without effecting the logical function of said circuit.

2. (original) The system of claim 1, wherein the circuit comprises an n-type transistor.

3. (original) The system of claim 1, wherein the circuit comprises an NMOS transistor.

4. (original) The system of claim 1, wherein the ESD protection system comprises a resistor.

5. (original) The system of claim 1, wherein the ESD protection system comprises a n-type transistor.

6. (original) The system of claim 1, wherein the ESD protection system comprises an NMOS transistor.

7. (original) The system of claim 1, wherein the ESD protection system comprises a p-type transistor.

8. (original) The system of claim 1, wherein the ESD protection system comprises an PMOS transistor.

9. (currently amended) A system comprising

a pad;

a circuit; and

means for protecting the circuit, connected between the pad and the circuit, configured to substantially eliminate ESD from flowing to the circuit from the pad without effecting the logical function of said circuit.

10. (original) The system of claim 9, wherein the circuit comprises an n-type transistor.

11. (original) The system of claim 9, wherein the circuit comprises an NMOS transistor.

12. (original) The system of claim 9, wherein the means for protecting comprises a resistor.

13. (original) The system of claim 9, wherein the means for protecting comprises a n-type transistor.

14. (original) The system of claim 9, wherein the means for protecting comprises an NMOS transistor.

15. (original) The system of claim 9, wherein the means for protecting comprises a p-type transistor.

16. (original) The system of claim 9, wherein the means for protecting comprises an PMOS transistor.

17. (currently amended) A system comprising

a circuit;

one of a NMOS transistor and a PMOS transistor; and

a pad,

wherein the one of the NMOS transistor and the PMOS transistor substantially eliminates ESD from flowing from the pad into the circuit without effecting the logical function of said circuit.